What is claimed is:

1. An electrically programmable three-dimensional memory (EP-3DM), comprising

a substrate circuit, said substrate circuit comprising a peripheral circuit, said peripheral circuit further comprising a plurality of data sense-amplifiers (S/A);

at least an EP-3DM level stacked on said substrate circuit, said EP-3DM level comprising a unit array, said unit array further comprising a plurality of EP-3DM cells, data-bit lines and data-word lines;

a plurality of inter-level connecting vias, said inter-level connecting vias connecting said data-bit line with said data S/A.

2. The EP-3DM according to claim 1, further comprising a first constant dc-source, and a plurality of first switches, each bit line in said unit array being connected to said first constant dc-source through a selected one of said first switches, all first switches associated with said unit array being controlled by a same first control signal.

3. The EP-3DM according to claim 1, further comprising a second constant dc-source, and a plurality of second switches, each word line in said unit array being connected to said second constant dc-source through a selected one of said second switches, all second switches associated with said unit array being controlled by a same second control signal.

4. The EP-3DM according to claim 1, wherein

said data S/A further comprises a data S/A-enable (SE) signal; and

said data S/A samples the voltage on said data-bit line when said SE signal is asserted.

5. The EP-3DM according to claim 4, wherein all data S/A in said unit array share a same data SE signal.

6. The EP-3DM according to claim 4, further comprising a first timing bit line and an associated first timing S/A, the SE signal for said first timing S/A being connected to a

constant dc-source, whereby the output from said first timing S/A eventually toggles said data SE signal and triggers the data sampling for said data-bit line.

7. The EP-3DM according to claim 4, further comprising a second timing bit line and an associated second timing S/A, the SE signal for said second timing S/A being connected to said data SE signal, whereby the output from said second timing S/A eventually toggles said data SE signal and stops the data sampling for said data-bit line.

8. The EP-3DM according to claim 1, further comprising a dummy-bit line, wherein

said data S/A is a differential S/A with a first input and a second input; and

said data-bit line is connected with said first input; and

said dummy-bit line is connected with said second input.

9. The EP-3DM according to claim 1, wherein

said EP-3DM level comprises a plurality of EP-3DM cells comprising 3D-ROM layer, the read voltage (V_R) for said EP-3DM cell being larger than the largest supply voltage for said EP-3DM.

10. The EP-3DM according to claim 9, further comprising a V_R-generating block in said peripheral circuit.

11. The EP-3DM according to claim 1, wherein the total number of data-bit lines in said unit array is larger than the total number of data-word lines in said unit array.

12. The EP-3DM according to claim 1 further comprising a programming circuit in said peripheral circuit, wherein

said programming circuit comprises a first and second sub-decoders, said first and second sub-decoders sharing a same input address; and

said unit array comprises a first and second memory cells, said first memory cell being connected to said first sub-decoder, said second memory cell being connected to said second sub-decoder.

13. The EP-3DM according to claim 1, further comprising a programming voltage (V_{pp})-input pad in said peripheral circuit, whereby said V_{pp}-input pad feeds an external V_{pp} to said unit array.

14. An electrically programmable three-dimensional cached memory (EP-3DcM), comprising

a substrate circuit, said substrate circuit comprising a peripheral circuit, an embedded RAM (eRAM) and a control block;

at least an electrically programmable three-dimensional memory (EP-3DM) level stacked on said substrate circuit, said EP-3DM level comprising a plurality of EP-3DM cells and address-selection lines, said EP-3DM level using said peripheral circuit for address decoding and data sensing;

a plurality of inter-level connecting vias, said inter-level connecting vias connecting said EP-3DM level with said peripheral circuit;

wherein, the output of said peripheral circuit is connected with said eRAM, and said control block controls the data flow between said EP-3DM level and said eRAM.

15. The EP-3DcM according to claim 14, wherein said peripheral circuit further comprises a column decoder, said column decoder selecting a group of outputs from said EP-3DM level and feeding said group of outputs to said eRAM.

16. The EP-3DcM according to claim 15, wherein said control block provides incremental column addresses to said column decoder during a read cycle.

17. An electrically programmable three-dimensional memory (EP-3DM), comprising

a substrate circuit, said substrate circuit comprising an embedded ROM (eROM) and a plurality of multiplexors;

at least an electrically programmable three-dimensional memory (EP-3DM) level stacked on said substrate circuit, said EP-3DM level comprising at least a defective

structure selected from a defective EP-3DM cell, a defective word line and a defective bit line;

a plurality of inter-level connecting vias, said inter-level connecting vias connecting said EP-3DM level with said substrate circuit;

wherein, the output for said EP-3DM is selected from said EP-3DM level and said eROM by said multiplexors.

18. The EP-3DM according to claim 17, wherein said eROM stores the row address, column address and correctional bit for said defective EP-3DM cell.

19. The EP-3DM according to claim 17, wherein said eROM stores the row address and correctional bits for all EP-3DM cells on said defective word line.

20. The EP-3DM according to claim 17, wherein said eROM stores the column address and correctional bits for all EP-3DM cells on said defective bit line.